Am79R79 Ringing SLIC Device Technical Overview

AMD

Application Note

The Am79R79 Ringing Subscriber Line Interface Circuit (SLIC) device is designed to provide direct generation of the ringing voltage used in short loop applications such as Fiber-in-the-Loop, Radio-in-the-Loop, hybrid fiber/coax, and video telephony, as well as the BORSHT functions of other AMD SLIC devices. In meeting key ringing requirements of TR909, the power supply for ringing is reduced to 70 V.

Am79R79 Ringing SLIC Device Features

The Am79R79 Ringing SLIC device has the necessary circuitry to generate the ringing voltage for short loop applications. It also includes on-chip ring trip detection. As with other AMD SLIC devices, the Am79R79 Ringing SLIC device has programmable features such as current feed, two-wire impedance, overhead, and loop detect threshold. One of two battery voltages can be selected. Typically, the most negative battery supply (V_{BAT1}) is used for ringing and other on-hook states, and the other, less negative battery supply (V_{BAT2}) is used for off-hook states. To prevent excessive voltage from appearing on the telephone line, the Am79R79 Ringing SLIC device provides anti-saturation guards that are adjustable for each battery supply. Digital inputs provide the ability to set the Am79R79 Ringing SLIC device into the eight states of operation supported. The characteristics of those states match other AMD SLIC devices, except in the Ringing state.

On-Chip Ringing

A ringing generator must provide an adequate signal at the linecard to have sufficient voltage across the telephone handset to cause it to ring (typically 40 V root-mean-square (rms)). The level of the required ringing signal generated at the linecard will depend on the loop resistance and the ringing load. The North American ringing load requirement of five REN (ringer equivalent number)—approximately 1400 Ω—is among the world's most stringent. This ringing load assures a sufficient level for nearly all applications, since many international specs require only three REN to be driven.

Traditionally, the central office (CO) has been required to be able to drive five REN through 1500 Ω lines to 40 Vrms. This long line requires a ringing voltage of about 90 Vrms at the linecard. An additional constraint was multiparty ringing, which requires that –48 V and the superimposed AC ringing signal be applied to tip or ring for ringing and ring trip detection. The Am79R79 Ringing SLIC device takes advantage of the less stringent requirements for short loop applications and uses a new ringing technique to reduce the ringing supply requirements to 70 V.

Table 1 shows the maximum loop resistance and ringing voltage crest factor for LSSGR, DLC, and FITL. The LSSGR maximum loop length of 1500 Ω requires a ringing voltage in excess of 90 Vrms at the linecard to supply the required 40 Vrms at the handset. With the 70 Ω maximum loop resistance for FITL, a lower ringing voltage will suffice since the voltage drop in the line will be considerably less. Assuming a 150 Ω series resistance total in the linecard, 70 Ω in the line, and 1400 Ω of ringing load, only about 46 Vrms is needed at the SLIC A and B leads to get 40 Vrms at the telephone.

The crest factor (CF) of a waveform is the ratio of the peak (pk) value to its root-mean-square value. Thus, a waveform with a higher crest factor will require a higher peak value to get the same rms value. A sine wave has a crest factor of 1.414, while a square wave has a crest factor of 1. A 1 Vpk square wave will have the same rms value as a 1.414 Vpk sine wave. TR909 requires a ringing voltage of 40 Vrms at the handset with a crest factor between 1.2 and 1.6. To minimize the peak voltage required, and thus get the most out of the available supplies, the Am79R79 Ringing SLIC device generates a trapezoidal waveform that has a crest factor that can be adjusted between 1.1 and 1.6. A crest factor of 1.25 would typically provide a crest factor within the requirements and provide some margin. For a 40 Vrms ringing signal at the handset, a trapezoidal waveform with a crest factor of 1.25 would require a ringing signal of 50 Vpk. If it were sinusoidal, it would require over 56 Vpk. An advantage of the sinusoidal signal is that its harmonic content is limited. This is important when wires run in a common bundle for a long distance and can couple into each other due to the capacitance between pairs. However, for short loop applications, wire pairs run alongside each other for a limited distance, so the greater harmonic content of the trapezoidal waveform can be tolerated by the inherently lower crosstalk of the short lines.

Most phone ringing is unbalanced where the ringing voltage is applied to the ring lead, as shown in Figure 1a.

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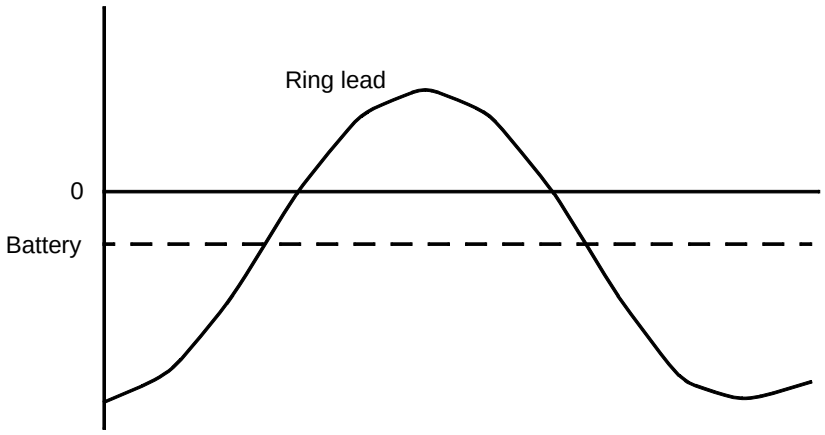
Table 1. Crest Factor Requirements for Various Bellcore Specs

	Loop Resistance (Max)	Ring Voltage Crest Factor (Spec)
CO (LSSGR)	1500 Ω	1.35–1.45
DLC (TR57)	900 Ω	1.2–1.6
FITL (TR909)	17 Ω[1]	1.2–1.6

Note:
1. Specified as 500 feet of 22 American Wire Gauge (AWG) at 65°C.



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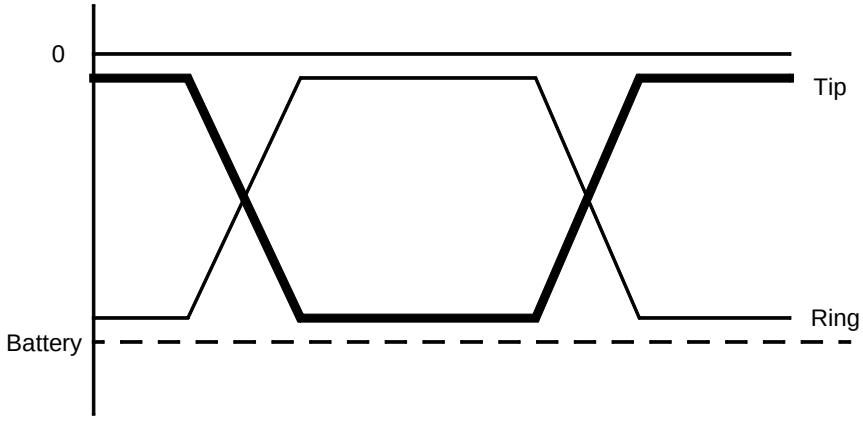
a. Sinusoidal Unbalanced Ringing



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b. Trapezoidal Balanced Ringing

Figure 1. Unbalanced and Balanced Ringing

Typical ringing requirements are for an AC signal of greater than 86 Vrms superimposed on –48 V. This allows the use of a single-ended ringing generator, which allows for multiparty ringing. Since multiparty ringing is not a requirement of short loop applications, the constraint of a single-ended ringing voltage applied to only tip or ring does not apply. To get 45 Vrms at the linecard with a 75 V battery is not possible with unbalanced ringing. Even a 70 V peak-to-peak (pk-pk) square wave would only result in 35 Vrms, and it has a crest factor of 1, not the 1.2 minimum. With balanced ringing, a metallic (differential) signal appears across A and B leads, as shown in Figure 1b. It can generate a ringing voltage with a peak value equal to the battery voltage, minus the amplifier overhead of 5 V. With a typical 70 V battery, minus the 5 V of overhead, the peak value of ringing voltage is 65 V. With a crest factor of 1.25, the ringing voltage at the SLIC A and B leads is 52 Vrms.

DC Offset During Ringing

Traditionally, DC offset between the tip and ring leads has been necessary for ring trip detection. The reason for this has been the AC vs. DC impedance seen from the CO in on-hook and off-hook states. For example, for a LSSGR line with 10 kΩ minimum line leakage, the on-hook and off-hook AC and DC impedance is shown in Table 2.

Table 2. On-Hook vs. Off-Hook Impedances, LSSGR

Central Office	AC	DC
On-hook	1.23 kΩ to infinity	10 kΩ to infinity
Off-hook	0 Ω to 1.93 kΩ	0 Ω to 1.93 kΩ

The AC impedance range overlaps on-hook vs. off-hook, making it impossible to reliably detect ring trip over all possible conditions. However, the DC on-hook/off-hook impedance ratio is over five worst case, making detection relatively easy. Table 3 shows the same data for TR909.

Table 3. On-Hook vs. Off-Hook Impedances, TR909

FITL/TR909	AC	DC
On-hook	1.23 kΩ to infinity	10 kΩ to infinity
Off-hook	0 Ω to 500 Ω[1]	0 Ω to 500 Ω

Note:

1. This assumes a loop resistance of 70 Ω and not the actual spec of 17 Ω, which gives extra margin to the spec.

While the DC on-hook/off-hook impedance ratio is over 20, the AC ratio is over 2. By setting an AC threshold to about 900 Ω, there is a sufficient margin for reliable detection. Since AC detection is possible, there is no need for a DC offset for ring trip detection; therefore, the ringing voltage does not require an offset between the tip and ring leads. This allows the AC ringing voltage to use the entire supply for the AC waveform.

Implementation

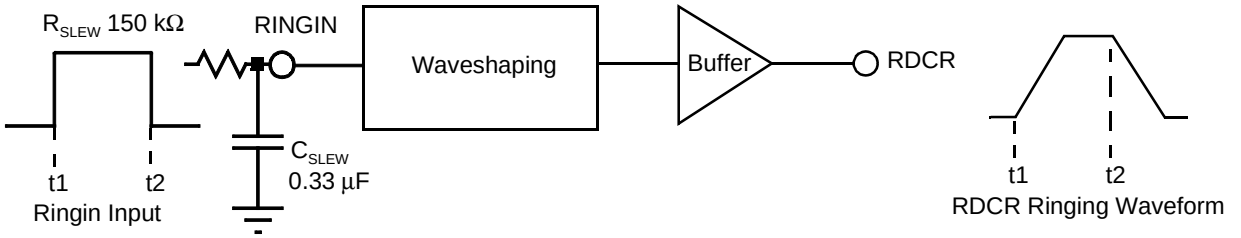

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Figure 2. Ringing Input

RINGING FEED

The ringing feed circuitry generates a trapezoidal ringing voltage from a square wave signal applied to the RINGIN pin. This circuitry along with the external RC network at RINGIN controls the crest factor of the ringing signal.

The CMOS-compatible reference input, RINGIN, is shown in Figure 2. The input to this must be a 50% duty cycle square wave applied to the external resistor-capacitor network made up of R_{SLEW} and C_{SLEW}, and needs to go as close as possible to V_{CC} and GND. The V_{CC} used to generate the square wave should be the same used for the SLIC V_{CC} to avoid offsets between the SLIC internal reference and the signal. R_{SLEW} and C_{SLEW} are selected to get the rate of change needed for a given crest factor through the waveshaping circuitry. The choice of resistor R_{DCR}, which connects to pin RDCR, determines the current to drive to the A and B amplifiers. The current can be chosen for a desired peak value for a given application. This is discussed in more detail in the *Ringing Circuitry* section on page 5 and in the appendix. The maximum voltage on RDCR is ±3 V. The characteristic is shown in Figure 3; this shows that there is a peak current available, $I_{RINGLIM,}$ that will drive into a short circuit, and into an open circuit the voltage will increase to V_{BAT1} – 3 V.

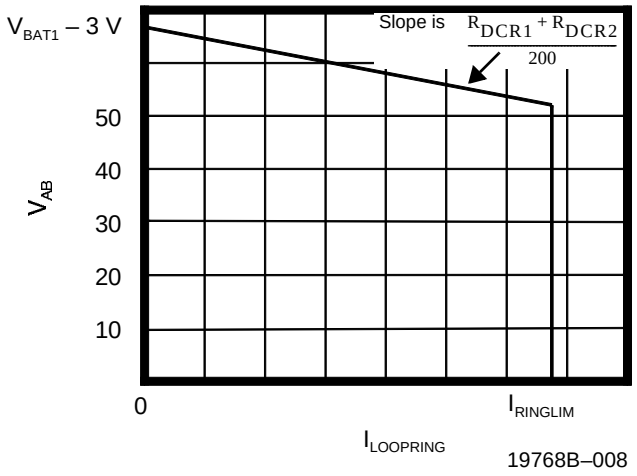

Figure 3. Ringing Feed

CREST FACTOR

To calculate the appropriate values for an arbitrary crest factor, it is necessary to discuss the input circuitry characteristics. The transition region of the input is about 0.52 V. The equation for rate of change of voltage across a capacitor with a constant current through it is

$$\Delta t = \frac{C \bullet \Delta V}{I}$$

For the 0.52 ΔV that the input moves, it is an adequate approximation to assume there is a constant current in C_{SLEW}. A CMOS-compatible input will go nearly to the supplies, so the current through R_{SLEW} will be about 2.5 V/R_{SLEW}. Substituting the current through R_{SLEW}, the value of ΔV, and C_{SLEW} instead of C into the above equation yields the following result:

$$\Delta t = \frac{C_{SLEW}(0.52\ V)}{(2.5\ V)/(R_{SLEW})} = 0.214 \bullet R_{SLEW} \bullet C_{SLEW}$$

This represents the time spent in the Linear mode and is the transition time of the ringing waveform. The trapezoidal waveform can be considered a square wave part that has a crest factor of 1 with two added triangular sections (the leading and trailing transition times) having a crest factor of 1.73. The total time of the triangular portions will be twice the Δt in the above equation. The square wave time will be the period of the ringing waveform, minus the total time for the triangular portions.

To calculate the crest factor, the rms value of the ringing waveform must be found. Since the peak value will appear in the numerator and denominator, and will cancel out, the equation can be normalized to an amplitude of unity to simplify the equation. The rms value of the overall waveform can be calculated by taking the rms value of the segments that make up the trapezoidal waveform and combining them. There is one triangular segment making up the leading edge and another making up the trailing edge, both of which have as their portion of the overall waveform the time period equal to Δt in the equation above, which is 0.214 • R_{SLEW} • C_{SLEW}. The triangular segments have an rms value of 0.577. The other part of the waveform is a square wave that has an rms value of 1 and a period of the overall period, minus the amount of time the triangular segments take up. The rms value of the waveform can be found by taking the contribution of the segments, and dividing by the total period (Per), as illustrated by the following equation:

$$\text{Trapezoid rms} = \frac{(2 \bullet 0.214 \bullet R_{SLEW} \bullet C_{SLEW}) \bullet 0.577 + (Per - (2 \bullet 0.214 \bullet R_{SLEW} \bullet C_{SLEW})) \bullet 1}{Per}$$

The crest factor is the inverse of this, which can be simplified as follows:

$$CF = \frac{Per}{Per - (0.176 \bullet R_{SLEW} \bullet C_{SLEW})}$$

Rearranging to solve for $R_{SLEW}C_{SLEW}$ for a given crest factor yields the equation:

$$(R_{SLEW} \bullet C_{SLEW}) = \frac{(CF \bullet Per) - Per}{CF \bullet 0.176}$$

For a crest factor of 1.25 at a RINGIN frequency of 20 Hz, $R_{SLEW}C_{SLEW}$ is 56.8 ms.

Figure 4 shows the ringing and DC Feed control loop for the Am79R79 Ringing SLIC device. RSN is a virtual ground. The current output at the A and B leads is 1000 times the current into the RSN pin, I_{RSN}.

RINGING CIRCUITRY

In the Ringing state, VTX and RDC are inactive and RDCR is active. Ignoring the contribution of the signal V_{RX}, since it is not applied during ringing, and keeping in mind that the loop current is 1000 times I_{RSN},

$$I_{LOOPRING} = \frac{V(RDCR)}{R_{DCR1} + R_{DCR2}} \bullet 1000$$

The series resistance of the ringing feed, R_S, is

$$R_S = \frac{R_{DCR1} + R_{DCR2}}{200}$$

The ringing feed needs a time constant between 15 µs and 150 µs, which puts the pole between 1 kHz and 10 kHz. This will not interfere with the ringing signal, but will attenuate higher frequencies. Also, if the time constant of the ringing feed is too slow, it will increase the crest factor since it will slow the ringing signal in addition to the $R_{SLEW}C_{SLEW}$ time constant. The time constant in the Ringing state, τ_{RING} is the following:

$$\tau_{RING} = \frac{R_{DCR1} \bullet R_{DCR2}}{R_{DCR1} + R_{DCR2}} \bullet C_{DCR}$$

$R_{DCR1} + R_{DCR2}$ determines the total current available during ringing. For this example, it is assumed that the ringing load can be as low as 1.23 kΩ. To drive this to 40 Vrms requires 33 mArms, which is 41 mA peak, assuming a crest factor of 1.25. RDCR will drive to a maximum voltage of 3 V. If we assume a desired maximum drive of 100 mA, the maximum current into RSN would have to be 100 µA. Therefore, $R_{DCR1} + R_{DCR2}$ must be at most 30 kΩ. Setting them equal, they would be 15 kΩ each. C_{DCR} should be chosen for a time constant of 15 µs–150 µs; a 2 nF to 20 nF cap will do.

The ringing signal drives the A and B leads alternately positive and negative to the supply rails. When RINGIN is high, A is closest to ground and B is near V_{BAT1}; this is the DC condition closest to normal polarity operation. Thus, it is important to synchronize the shift from the Ringing state to the normal Active state with the time period that RINGIN is high to minimize any switching transients that may occur, and to minimize glitches on loop and ring trip detect when changing states.

RING TRIP

The ring trip threshold is defined as the resistance on the loop which causes the detect output (DET) to pulse low momentarily each ringing cycle. This will require system level debouncing. Figure 5 shows the ring trip and loop detect circuitry. The loop current is sensed and scaled to $|I_A+I_B|/300$. This current is replicated twice, and sent to both the RTRIP1 pin and the RD pin. The external components on the RTRIP1 pin determine the ring trip characteristics. R_{RT1} is an external resistor whose function is to set the threshold for ring trip detection. The 15 µA current source is provided to keep the RTRIP1 pin slightly negative so that the RTRIP1 node cannot inadvertently be positive when the Ringing state is entered. This would lead to a momentary false ring trip indication. The comparator for ring trip is referenced to ground. R_{RT2} will have 0 V across it at that time, so it is not a factor in setting the ring trip threshold. Therefore, to select R_{RT1}, use the following equation:

$$\left(\frac{|I_{LOOP}|}{300} - 15\ \mu A\right) \bullet R_{RT1} = V_{BAT1}$$

I_{LOOP} is equal to V_{AB} divided by the total resistance in the loop. This resistance is made up of fuse resistors R_F, the series resistance of the Am79R79 Ringing SLIC device R_S, and the desired ring trip resistance R_{LRT}. V_{AB} for this case is about V_{BAT1} – 3.5 V. Including the filtering of the signal by taking into account the crest factor CF gives:

$$R_{RT1} = 300 \bullet CF \bullet \frac{V_{BAT1}}{Vbat - 3.5 - (15\ \mu A \bullet 300 \bullet CF \bullet (R_{LRT} + R_S + 2R_F))} \bullet (R_{LRT} + R_S + 2R_F)$$

R_{RT1} will always connect to V_{BAT1}, since R_{RT1} is only connected in the Ringing state. For a typical application, V_{BAT1} is 70 V, R_S is 150 Ω, R_{LRT} is chosen for 900 Ω, CF is 1.25, and R_F is 40 Ω, giving a value for R_{RT1} of 503 kΩ. This is rounded to 510 kΩ. R_{RT1} is switched on-chip to conserve power. With a battery of 70 V, power dissipated in the resistor would be 11 mW.

R_{RT2} and C_{RT} provide filtering for ring trip and are selected for a time constant of approximately 18 ms. R_{RT2} should be selected to keep the voltage on the RTRIP1 pin within ±3 V. The most likely problem would be to select a large value of R_{RT2} and, during ringing, have R_{RT1} pull down towards V_{BAT1}. To use an example, if R_{RT2} were 50 kΩ, R_{RT1} 450 kΩ, and V_{BAT1} 70 V during ringing with no ringing current, RTRIP1 would be –7 V, leading to erratic operation. A value of 12 kΩ for R_{RT2} is a suitable choice for nearly all applications.

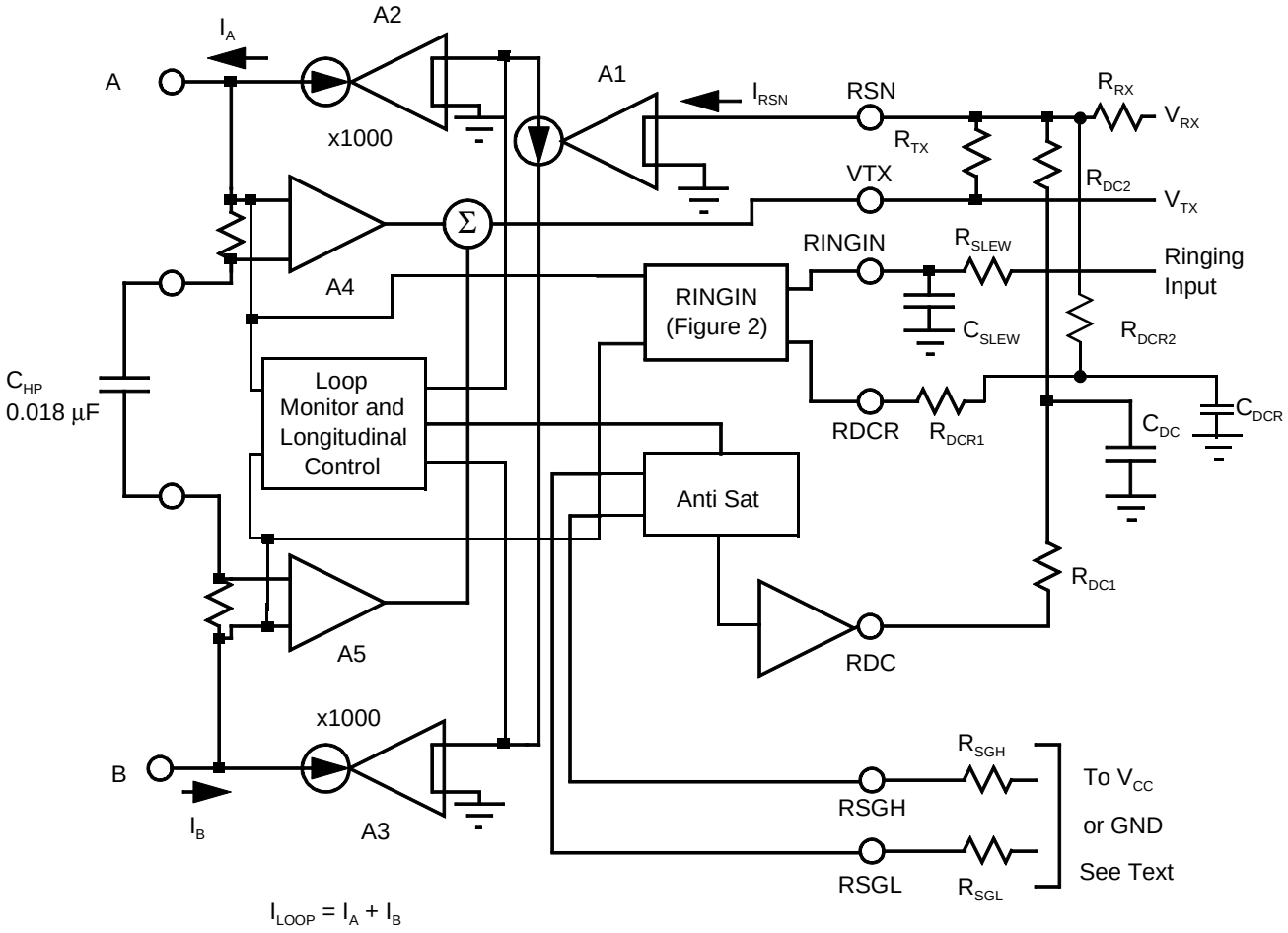

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Figure 4. Ringing and DC Feed

DC FEED

During the Active state, RDCR is open circuited and VTX and RDC are active. I_{RSN} is the total of the current flowing in R_{TX}, the resistors R_{DC1} and R_{DC2}, and R_{RX}. The longitudinal control loop senses V_{LONG}, defined as:

$$V_{LONG} = \frac{V_A - V_B}{2},$$

and then compares it to $V_{BATX}/2$ and adjusts the longitudinal voltage to be $V_{BATX}/2$. V_{BATX} is the battery voltage selected by the state or B2EN.

To find the DC bias, V_{RX} is assumed to be zero so that there is no contribution from the signal input. Also, for this analysis, it is assumed that there is no metallic input signal from the line, and therefore VTX will be zero. DC loop current will be determined by the voltage on RDC and by the resistance connected from RDC to RSN, which is R_{DC1} plus R_{DC2}. The current into RSN is as follows:

$$I_{RSN} = \frac{V(RDC)}{R_{DC1} + R_{DC2}}$$

Assuming that V_{AB} stays out of the anti-sat region, RDC is a fixed reference of 2.5 V. Since $I_{LOOP} = 1000 \bullet I_{RSN}$,

$$I_{LOOP} = \frac{2500}{R_{DC1} + R_{DC2}}$$

For a typical loop current of 25 mA, $R_{DC1} + R_{DC2}$ would be 100 kΩ. The capacitor C_{DC} is set for a DC loop time constant with R_{DC1} and R_{DC2} of 16 ms to 30 ms. The DC loop time constant, τ_{DC}, is defined by the following equation:

$$\tau_{DC} = \frac{R_{DC1} \bullet R_{DC2}}{R_{DC1} + R_{DC2}} \bullet C_{DC}$$

Equal values of R_{DC1} and R_{DC2} will result in the smallest C_{DC}. Using the above equation, $R_{DC2} = R_{DC1} = 50$ kΩ and $C_{DC} = 0.82$ µF, results in a time constant of 20 ms. The tolerance on this time constant is not critical; ±30% is adequate.

LOOP DETECT

Loop detect in the Active, OHT, and Standby states is determined by the external resistor connected to pin RD, R_D. For Active and OHT states, the loop detect status is determined by the total loop resistance. As shown in Figure 5, a current proportional to the loop current flows into the R_D resistor, and establishes a corresponding voltage into the loop detect comparator. In the Active and OHT states, the comparator's reference voltage, REF, is dependent upon V_{AB} divided by a reference voltage determined by the battery selected by B2EN, called BREF in the equations following. Since loop resistance is defined by tip/ring voltage divided by loop current, the result is a threshold comparison of loop resistance. For the Standby state, the comparator's reference, REF, is a constant voltage and the comparator detects at a current threshold established by the R_D resistor only. Since the Standby state feed is resistive, the loop current then becomes a function of battery voltage as well as loop resistance. The Standby state loop detect status is therefore also dependent upon the battery voltage.

In the Active and OHT states, the comparator for the loop detect has a reference determined by V_{AB} divided by BREF. This leads to the following equation:

$$\frac{|I_{LOOP}|}{300} \bullet R_D = \frac{V_{AB}}{BREF}$$

I_{LOOP} is V_{AB} divided by the total resistance on the loop. This resistance is made up of the fuse resistors R_F, line series resistance R_{SL}, and desired loop resistance for loop detect threshold R_{LTH}, which results in the following equation:

$$\frac{|V_{AB}|}{(R_{LTH} + R_{SL} + 2R_F) \bullet 300} \bullet R_D = \frac{V_{AB}}{BREF}$$

A simplified version of this equation, grouping constants, is as follows:

$$R_D = (R_{LTH} + R_{SL} + 2R_F) \bullet SCALE$$

In terms of R_{LTH}, the equation for Active and OHT loop detect for V_{BAT1} and V_{BAT2} is:

$$R_{LTH} = \frac{R_D}{SCALE} - R_{SL} - 2R_F$$

Table 4 shows the value of SCALE for the two batteries. Using 100 Ω for R_{SL}, 100 Ω for $2R_F$, plus a desired loop detection resistance R_{LTH} of 5 kΩ and a SCALE of 12.67 for V_{BAT1} results in 66 kΩ for R_D.

Table 4. SCALE Value vs. Battery Selected

Battery Selected	SCALE
V_{BAT2}	11.37
V_{BAT1}	12.67

In Standby state, the A and B pins are connected to the supplies through approximately 200 Ω each. The switches that connect the resistors require about 3 V of overhead. The B amplifier has a 7 V zener in series with V_{BAT1} in the Standby state, so the A and B amplifiers have a total of 10 V voltage drop from V_{BAT1} to the open circuit voltage. When in the Standby state, much of the internal circuitry is shut off to minimize power dissipation. The circuitry that remains active detects the loop current, not resistance, and the detect level is set by

$$R_D \quad \frac{915(R_{LTH} + 2R_F + 400 + R_{SL})}{|V_{BAT1}| - 10}$$

In terms of R_D, the equation for R_{LTH} in Standby state is

$$R_{LTH} = \frac{R_D \bullet (|V_{BAT1}| - 10)}{915} - 400 - 2R_F - R_{SL}$$

R_{LTH} is chosen to be greater than the phone off-hook resistance of about 500 Ω and less than the expected leakage resistance of 10 kΩ, so it is desirable to set R_{LTH} at about 5 kΩ. Choose R_{LTH} using the equation for Active and OHT loop detect with SCALE value of 12.67 (V_{BAT1} selected) and then calculate the resulting threshold resistance in the other states. R_D must be greater than 56 kΩ to ensure that, at the lowest possible specified Standby current, there still will be a detect. It is important that the detect threshold is set so that a detect in one state will be a detect in the next state, which is done automatically in the Am79R79 Ringing SLIC device. From the example above, R_{LTH} for Active V_{BAT1} was 5 kΩ with R_D of 66 kΩ. R_{LTH} for Active V_{BAT2} would then be 5.6 kΩ from the equation using the SCALE for V_{BAT2}. For the Standby state, calculating R_{LTH} using the conditions stated above and a BAT1 of 70 V, results in a Standby threshold of 3.7 kΩ; with a 50 V BAT1, it would be even lower at 2.3 kΩ. In normal operation, the linecard circuit state could go from Standby to Active V_{BAT2}. R_{LTH} is 3.7 kΩ in Standby and 5.6 kΩ in Active V_{BAT2}, so there still would be a valid detect after the state transition since the detect in Standby would have to be 3.7 kΩ or less, and the 5.6 kΩ threshold in Active V_{BAT2} would detect the load that is less than 3.7 kΩ. The same is true going from Active V_{BAT1} to Active V_{BAT2}; the threshold goes from 5 kΩ to 5.6 kΩ, again ensuring a valid detect, and no possibility of oscillation exists between states. Upon the completion of the call, the line goes to a high impedance, and the state would change from Active V_{BAT2} to either Standby or Active V_{BAT1}. Active V_{BAT2} detects at a higher resistance than the other two states, and thus prevents indicating an on-hook condition while the other state indicates an off-hook condition, again preventing oscillation between states.

ANTI-SAT CHARACTERISTICS

DC Feed characteristics are shown in Figure 6. With a given loop current, the voltage across the loop can increase to the anti-sat threshold value V_{ASL} for the low battery voltage V_{BAT2}, or V_{ASH} for the high battery voltage V_{BAT1}. Then the apparent feed synthesis loop gain is increased and the apparent output resistance decreases. The output voltage increases at a lower rate with increasing loop resistance, helping to keep the amplifiers in a linear region even though they are near the supplies. The two battery voltages have a separate resistor to adjust anti-sat characteristics: R_{RSGH} to adjust V_{ASH}, and R_{SGL} to set V_{ASL}. R_{SGL} sets V_{ASL}; however, V_{ASH} is dependent on both R_{SGH} and V_{ASL}. R_{SGH} and R_{SGL} can independently connect to either V_{CC} to decrease the knee voltage, or to ground to increase the knee voltage.

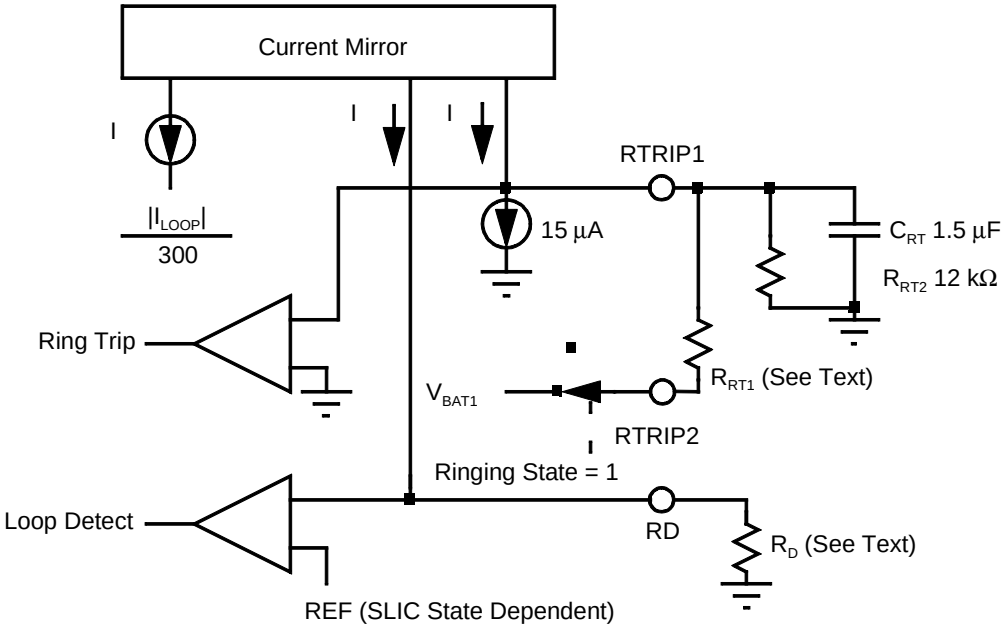

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Figure 5. Ring Trip and Loop Detect

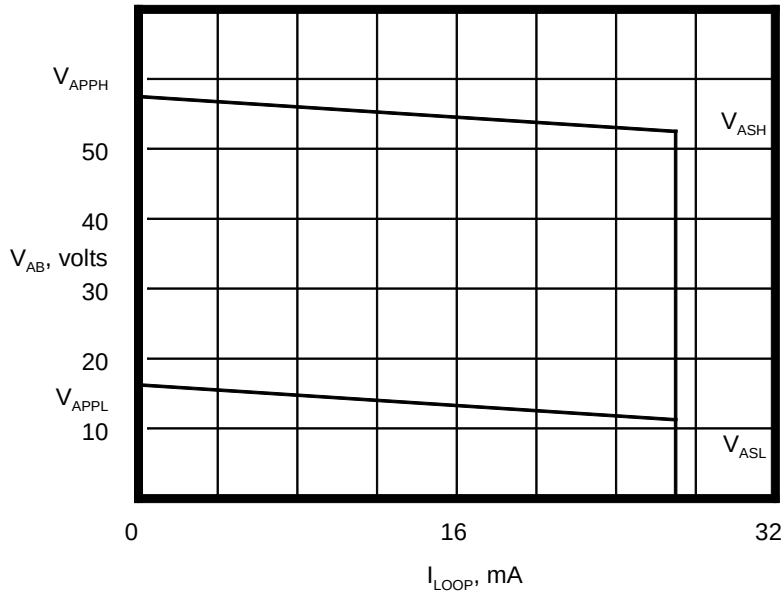

Figure 6. DC Feed

The low battery apparent voltage, V_{APPL}, is given by this equation:

$$V_{APPL} = 4.17\ V + V_{ASL}$$

When in the resistive region, the current in the loop is defined by this equation:

$$I_{LOOP} = \frac{V_{APPL}}{\left(\frac{R_{DC1} + R_{DC2}}{600}\right) + 2R_F + R_{LOOP}}$$

This equation is valid only in the resistive region, which means R_{LOOP} is sufficiently large so that the part is in the anti-sat region, and I_{LOOP} is less than the designed value for the constant current region. When R_{SGL} is connected to ground to increase the knee voltage, V_{ASL} is given by the following equation:

$$V_{ASL} = \frac{1000 \bullet (104 \bullet 10^3 + R_{SGL})}{6.72 \bullet 10^6 + 80 \bullet R_{SGL}}$$

Typically, designs require a target value of V_{ASL} and solve for R_{SGL}, so rearranging the equation yields the following:

$$R_{SGL} = \frac{V_{ASL} \bullet 6.72 \bullet 10^6 - 104 \bullet 10^6}{1000 - (80 \bullet V_{ASL})}$$

When R_{SGL} is connected to V_{CC} to decrease the knee voltage, V_{ASL} is given by the equation:

$$V_{ASL} = \frac{1000 \bullet (R_{SGL} - 56 \bullet 10^3)}{6.72 \bullet 10^6 + (80 \bullet R_{SGL})}$$

Rearranging to solve for R_{SGL} gives this equation:

$$R_{SGL} = \frac{V_{ASL} \bullet 6.72 \bullet 10^6 + 56 \bullet 10^6}{1000 - (80 \bullet V_{ASL})}$$

When R_{SGL} is connected to V_{CC}, it must have a value greater than 100 kΩ.

V_{APPH} has the same form as V_{APPL}, as shown in the following equation:

$$V_{APPH} = 4.17\ V + V_{ASH}$$

Loop current in the resistive region is determined by this equation:

$$I_{LOOP} = \frac{V_{APPH}}{\left(\frac{R_{DC1} + R_{DC2}}{600}\right) + 2R_F + R_{LOOP}}$$

V_{ASH} follows the equation:

$$V_{ASH} = V_{ASHH} + V_{ASL}$$

The value of V_{ASHH} depends on whether R_{SGH} is connected to V_{CC} or to ground. For the case where R_{SGH} is connected to ground, the equation is:

$$V_{ASHH} = \frac{1000 \bullet (70 \bullet 10^3 + R_{SGH})}{1.934 \bullet 10^6 + (31.75 \bullet R_{SGH})}$$

Rearranging to solve for R_{SGH} with a known V_{ASHH} gives the equation:

$$R_{SGH} = \frac{V_{ASHH} \bullet 1.934 \bullet 10^6 - 70 \bullet 10^6}{1000 - (31.75 \bullet V_{ASHH})}$$

With R_{SGH} connected to V_{CC}, V_{ASHH} is given by the following equation:

$$V_{ASHH} = \frac{1000 \bullet (2.75 \bullet 10^3 + R_{SGH})}{1.934 \bullet 10^6 + (31.75 \bullet R_{SGH})}$$

Rearranging to solve for R_{RSGH} with a known V_{ASHH} yields the equation:

$$R_{SGH} = \frac{V_{ASHH} \bullet 1.934 \bullet 10^6 - 2.75 \bullet 10^6}{1000 - (31.75 \bullet V_{ASHH})}$$

To calculate V_{ASH}, V_{ASL} must first be determined. As a first example, the values of V_{ASL} and V_{ASH} with pins RSGH and RSGL open circuit can be found in a straightforward manner. An open circuit is an infinite resistance; substituting that into the equations gives V_{ASL} equal to 12.5 V, and V_{ASHH} equal to 31.5 V. V_{ASH}, as defined earlier, is the sum of V_{ASHH} and V_{ASL}, so V_{ASH} is 44 V.

For a second example, assume a design needs V_{ASL} of 15 V and V_{ASH} of 40 V. Since V_{ASL} is increased, choose the equation that has R_{SGL} connected to ground. Solving yields R_{SGL} equal to 16 kΩ. As the resistance decreases, V_{ASL} increases. The maximum V_{ASL} occurs when R_{SGL} is zero, which is 15.47 V. To calculate V_{ASH}, subtract V_{ASL} of 15 V from the target V_{ASH} of 40 V to get V_{ASHH} of 25 V. The minimum V_{ASHH} from the equation for V_{ASHH} with R_{SGH} connected to V_{CC} is (with R_{SGH} of zero) 1.42 V, so the target is achievable. R_{SGH} of 221 kΩ will achieve V_{ASHH} of 25 V, so V_{ASH} will be 25 V plus 15 V or 40 V. When decreasing V_{ASL}, R_{SGL} must be 100 kΩ or greater.

BATTERY VOLTAGES

The Am79R79 Ringing SLIC device supports the selection of two battery voltages. V_{BAT1} is always connected to the substrate and must be the more negative battery with a value as low as –75 V. V_{BAT2} can range from –19.5 V to V_{BAT1}. Figure 7 shows the recommended configuration as well as the sense of the logic switch: if B2EN is a logic High, V_{BAT1} is selected; if it is Low, V_{BAT2} is selected. The diode isolation allows V_{BAT1} to override V_{BAT2} when the internal switch closes. When the switch opens, the diode to V_{BAT2} forward biases and V_{BAT2} is applied to the circuit. When in the Standby state, the Am79R79 Ringing SLIC device is internally connected to V_{BAT1}, so the selection of B2EN in the Standby state is irrelevant; the part will always connect to V_{BAT1} to meet the open circuit voltage requirements for FAX machines and MTU's.

VNEG

The circuitry driven by V_{NEG} includes a V_{EE} regulator which allows V_{NEG} to be driven by any voltage between –5 V and V_{BAT2}. It must connect to BAT2 on the supply side of the power supply diode because of the way that V_{BAT1} voltage can appear on that pin as described above. A resistor can be placed in series with the connection to limit on-chip power dissipation with a value chosen to be less than the voltage drop between BAT2 and –5 V with a 2 mA current.

LIGHTNING AND POWER CROSS

With the higher magnitude BAT1 voltage that the Am79R79 Ringing SLIC device allows, choice of a lightning/power cross protection device should be considered. The protection voltage should not be greater than 80 V to avoid exceeding the maximum limits of the process. For battery voltages below 65 V, a protection device with a fixed protection voltage of 80 V would provide sufficient margin for operation. However, above a 65 V BAT1, this may provide little margin, and a protection device that tracks battery and ground may provide a greater margin of safety.

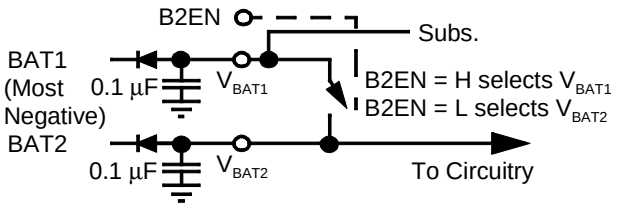

Figure 7. V_{BAT1} and V_{BAT2}

RELAY DRIVERS

The relay drivers RYOUT1 and RYOUT2 are provided to allow the driving of up to 75 mA per driver to energize a relay. To make these more versatile, the common emitter connection of the drivers are brought out to a pin. The drivers are transistors with internal snubber circuits. If an application does not need the relay drivers, they can be used to implement test functions as illustrated in Figure 8. With the addition of the external diode and the test load resistors, RYOUT1 is set up for loop continuity tests and RYOUT2 is set up for a ground-key test.

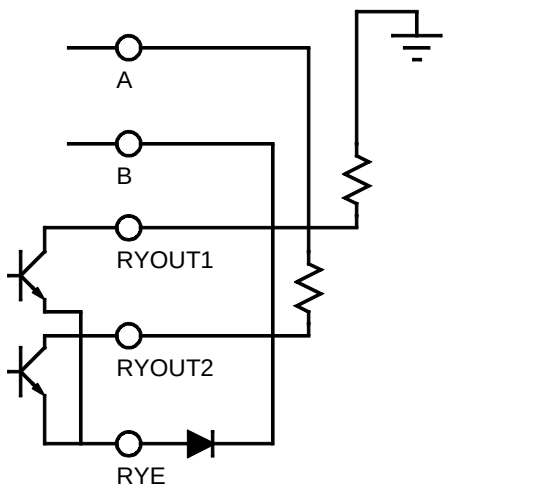

Figure 8. Using Relay Drivers for Test Loads

Appendix 1 Design Example

The Am79R79 Ringing SLIC device has two current limits that can be set independently. These user-defined current limits are for the ringing feed and the DC loop feed. The currents are set by connecting a network from RDC to RSN for the DC Feed, and a network from RDCR to RSN for the ringing feed. The equation that describes the DC loop current limit is

$$I_{LOOP} = \frac{2500}{R_{DC1} + R_{DC2}}$$

For the ringing feed, the current is

$$I_{LOOPRING} = \frac{V(RDCR) \bullet 1000}{R_{DCR1} + R_{DCR2}}$$

The maximum value of $I_{LOOPRING}$ occurs when V(RDCR) is at its peak value, which occurs at ±3 V. This current, called $I_{RINGLIM}$, is defined by the equation:

$$I_{RINGLIM} = \frac{3000}{R_{DCR1} + R_{DCR2}}$$

$I_{RINGLIM}$ is the current limited peak value of the ringing current. To get the rms value, $I_{RINGLIM}$ must be divided by the crest factor.

Values for I_{LOOP} and $I_{RINGLIM}$ must be chosen. A typical value is 25 mA for I_{LOOP} which gives a sufficient current to drive a phone with some extra for leakage and component tolerance. $I_{RINGLIM}$ can be as much as 100 mA when a strong drive is required for ringing. For ringing single phones, $I_{RINGLIM}$ can be reduced to 30 mA or below for applications requiring a minimum current draw from the supply. The ringing current limit should be set to at least 11 mA per REN. Setting the current limit also sets the Am79R79 SLIC device output resistance. Setting the current limit higher than 11 mA per REN reduces the output resistance but increases the peak current the power supply must be able to deliver into a short circuit. To minimize the size of C_{DC} and C_{DCR} it is best to make $R_{DC1} = R_{DC2}$ and $R_{DCR1} = R_{DCR2}$. With the above values and assuming 100 mA for $I_{RINGLIM}$, $R_{DC1} = R_{DC2} = 50\ k\Omega$ and, $R_{DCR1} = R_{DCR2} = 15\ k\Omega$.

The time constant for the DC loop is

$$\tau_{DC} = \frac{R_{DC1} \bullet R_{DC2}}{R_{DC1} + R_{DC2}} \bullet C_{DC} = 20\ \text{ms}$$

with the given values for R_{DC1} and R_{DC2}, C_{DC} = 820 nF.

This equation shows the ringing time constant:

$$\tau_{RING} = \frac{R_{DCR1} \bullet R_{DCR2}}{R_{DCR1} + R_{DCR2}} \bullet C_{DCR} = 15\ \mu s\ \text{to}\ 150\ \mu s$$

Using a τ_{RING} of 100 µs, $C_{DCR} \approx 12$ nF.

R_{RT1} should be calculated from the equation for R_{RT1} on page 5. The choice of $I_{RINGLIM}$ will have an effect on R_{RT1}. Any time the ringing current limit is changed, the value of R_{RT1} must also be changed. The value of R_{RT1} also is dependent on the chosen crest factor (CF), the battery V_{BAT1}, and the desired load at which the ringing will be detected (R_{LRT}). The ring detect threshold, R_{LRT}, will be the value at which the ringing is just detected. Since the ringtrip is only lightly filtered, this detect will glitch, especially near R_{LRT}. This value is typically chosen well away from the resistance presented by an off-hook phone, plus line resistance, plus fuse resistors. A phone is specified to be no more than 430 Ω off-hook, and the fuse resistors, plus line resistance may be a total of 70 Ω or more, so 500 Ω is an acceptable number to use. The ringing impedance of the load needs to be taken into account when setting the threshold. If driving a 5 REN load with a worst-case leakage resistance of 10 kΩ, then the ring impedance is about 1200 Ω. R_{LRT} should be selected about halfway between the off-hook resistance and the ringing impedance; 900 Ω would be a good value for a 5 REN load.

Table 5 shows three examples of I_{LOOP} and $I_{RINGLIM}$, and shows the resistor values needed.

Table 5. Design Examples for Various Conditions

Example	I_{LOOP}	$I_{RINGLIM}$	$R_{DC1} = R_{DC2}$	$R_{DCR1} = R_{DCR2}$	C_{DC}	C_{DCR}	R_D	R_{RT1}
1	25 mA	30 mA	50 kΩ	50 kΩ	820 nF	4 nF	66 kΩ	696 kΩ
2	25 mA	100 mA	50 kΩ	15 kΩ	820 nF	12 nF	66 kΩ	515 kΩ
3	40 mA	62.5 mA	31.5 kΩ	24 kΩ	1.2 µF	8.2 nF	66 kΩ	561 kΩ

R_{RT2} = 12 kΩ, C_{RT} = 1.5 µF, V_{BAT1} = –70 V, CF = 1.25, R_{LRT} = 900 Ω

If $R_{DCR1} + R_{DCR2}$ is greater than or equal to 100 kΩ, a single resistor can be used. The circuit configuration for this case is shown in Figure 9.

For the ringing feed, the current is

$$I_{RINGLIM} = \frac{3000}{R_{DCR}}$$

The calculation of DC loop current and time constant is the same as in previous examples.

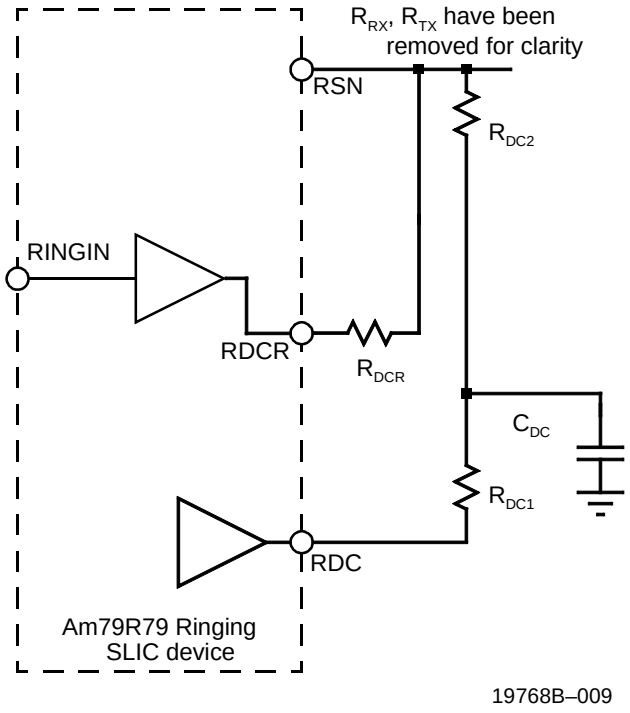

Figure 9. Alternate Networks for Ringing and Loop Current Settings